REMARKS

Claims 1-6 and 13-20 are pending in the present application. Claims 1, 3-5, 13, 15-17, 19 and 20 have been amended. Claims 7-12 have been canceled. Applicant respectfully reserves the right to file a divisional application including claims 7-12.

Information Disclosure Statement

An Information Disclosure Statement has been filed concurrently herewith. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement, and to confirm that the documents submitted therewith have been considered and will be cited of record in the present application.**

Claim Objections

Claims 1-6 and 13-20 have been objected to in view of the informalities listed at the top of page 3 of the Final Office Action dated July 29, 2005. Although Applicant does not necessarily agree with the Examiner's assertion that correction of the claims is necessary, claim 1 has been amended to feature "a thin silicon layer on the buried oxide layer...". Claim 13 has been amended in a somewhat similar manner to feature "an SOI layer on the BOX layer...". The Examiner is therefore respectfully requested to withdraw the objection to the claims.

Claim Rejections-35 U.S.C. 102

Claims 1-5, 13-17, 19 and 20 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Wakahara et al. reference (Japanese Patent Publication No. 2000-183355). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The full depletion SOI-MOS transistor of claim 1 includes in combination a substrate; a buried oxide layer; a thin silicon layer "on the buried oxide layer, the thin silicon layer including a channel region and an impurity diffused source/drain region"; an isolation layer; a gate insulation layer; a gate electrode; and a deposited polysilicon layer "on the impurity diffused source/drain region of the thin silicon layer, wherein the impurity diffused source/drain region and the deposited polysilicon layer together constitute a source/drain of a full depletion SOI-MOS transistor". Applicant respectfully submits that the Wakahara et al. reference as relied upon by the Examiner does not disclose these features.

In the full depletion SOI-MOS transistor of claim 1 as noted above, the impurity diffused source/drain region and the deposited polysilicon layer together constitute a source/drain of the transistor. As a result of using the deposited polysilicon layer, the problem of this layer of the source/drain condensing does not occur. Accordingly, a transistor with high reliability can be realized. Additionally, the advantages as described on page 5, line 21 through to page 6, line 1 of the present application may be realized.

The Examiner has primarily relied upon Fig. 11 of the Wakahara et al. reference

as meeting the features of claim 1. The Examiner has apparently interpreted thin film silicon layer 3 and selective silicon growth layer 13b respectively as the thin silicon layer and the polysilicon layer of claim 1. However, as described in paragraph [0029] of the English translation of the Wakahara et al. reference, layer 13b is a layer of selective silicon growth, not a deposited polysilicon layer as would be necessary to meet the features of claim 1. Accordingly, the Wakahara et al. reference as relied upon by the Examiner does not include an impurity diffused source/drain region and a deposited polysilicon layer that together constitute a source/drain of a full depletion SOI-MOS transistor as featured in claim 1. The Wakahara et al. reference does not provide a transistor with high reliability as in the present invention. Applicant therefore respectfully submits that the full depletion SOI-MOS transistor of claim 1 distinguishes over the Wakahara et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1-5, is improper for at least these reasons.

Also, since the Wakahara et al. reference as relied upon by the Examiner does not disclose a deposited polysilicon layer as would be necessary to meet the features of claim 1, the Wakahara et al. reference thus fails to meet the features of respective claims 3-5. Applicant therefore respectfully submits that this rejection, insofar as it may pertain to the claims 3-5, is improper for at least these additional reasons.

The full depletion SOI-MOS transistor of claim 13 includes in combination a substrate; a BOX layer; and SOI layer "on the BOX layer, the SOI layer including a channel region and an impurity diffused source/drain region"; an isolation layer; a gate

insulation layer; a gate electrode; and a deposited high mobility conductive layer "on the impurity diffused source/drain region of the thin silicon layer, wherein the deposited high mobility conductive layer contains polysilicon and wherein the impurity diffused source/drain region and the deposited high mobility conductive layer together constitute a source/drain of the full depletion SOI-MOS transistor".

Applicant respectfully submits that the full depletion SOI-MOS transistor of claim 13 distinguishes over the Wakahara et al. reference for at least somewhat similar reasons as set forth above with respect to claim 1. That is, Fig. 11 of the Wakahara et al. reference as primarily relied upon by the Examiner does not include a deposited high mobility conductive layer containing polysilicon, wherein an impurity diffused source/drain region and the deposited high mobility conductive layer containing polysilicon together constitute a source/drain of a transistor. The Wakahara et al. reference therefore fails to provide a transistor with high reliability as in the present invention. Applicant therefore respectfully submits that the full depletion SOI-MOS transistor of claim 13 distinguishes over the Wakahara et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 13-17, 19 and 20, is improper for at least these reasons.

Also, since the Wakahara et al. reference as relied upon by the Examiner does not disclose a deposited high mobility conductive layer containing polysilicon, the Wakahara et al. reference clearly fails to disclose the features of respective claims 15-17, 19 and 20. Applicant therefore respectfully submits that these claims distinguish

over the relied upon prior art for at least these additional reasons.

Claim Rejections-35 U.S.C. 103

Claims 6 and 18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Wakahara et al. reference in view of the Cheng et al. reference (U.S. Patent Application Publication No. 2002/0171107). Applicant respectfully submits that the Cheng et al. reference as relied upon by the Examiner does not overcome the above noted deficiencies of the Wakahara et al. reference. Applicant therefore respectfully submits that this rejection, insofar as it may pertain to claims 6 and 18, is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

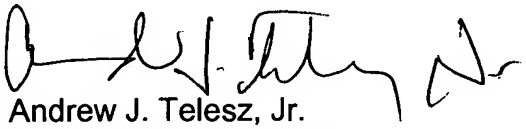
Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of two (2) months to December 29, 2005, for the period in which to file a response to the outstanding Office Action. The required fee of $450.00

should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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